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l1 and L2	28

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L3

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side by side

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result set

DB=USPT; PLUR=YES; OP=OR

<u>L3</u>	l1 and L2	28	<u>L3</u>
<u>L2</u>	header same (payload or data) same (control adj1 (path or bus))	198	<u>L2</u>
<u>L1</u>	node near10 network	21958	<u>L1</u>

END OF SEARCH HISTORY

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Terms	Documents
L3	0

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Query

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Set Name

result set

DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4

L3

0

L4

DB=USPT; PLUR=YES; OP=OR

L3

11 and L2

28

L3

L2

header same (payload or data) same (control adj1 (path or bus))

198

L2

L1

node near10 network

21958

L1

END OF SEARCH HISTORY

EAST - [Untitled1:1]

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Drafts
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Active
L1: (21958) node near10 ne
L2: (19) header same paylo
L3: (6) 11 and 12
Failed
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Tagged (0)
UDC
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Trash

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DBs USPAT Plurals
Default operator: OR Highlight all hit terms initially

BRS1 SAR Image Text HTML

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	21958	node near10 network	USPAT	2003/07/24 16:06			0
2	BRS	L2	19	header same payload same (control adj1 (path or	USPAT	2003/07/24 16:08			0
3	BRS	L3	6	11 and 12	USPAT	2003/07/24 16:08			0

Start EAST [Untitled1]

EAST - [Untitled1:1]

FileViewEditToolsWindowHelp

Drafts

Pending

Active

- L1: (21958) node near10 ne
- L2: (19) header same paylo
- L3: (6) 11 and 12

Failed

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11 and 12

BRS I...S&R...ImageTextHTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6311230 B1	20011030	11	System and method for cell switching with a peripheral	710/5	370/396; 710/119;	
2	<input type="checkbox"/>	<input type="checkbox"/>	US H001964 H	20010605	21	Resource management sub-system of a	370/419		
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5892535 A	19990406	69	Flexible, configurable, hierarchical system for	725/36	345/716; 725/91;	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5862136 A	19990119	59	Telecommunications apparatus and method	370/395.4	370/375; 370/376	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5841771 A	19981124	65	Telecommunications switch apparatus and method for	370/360	370/375; 370/383	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5745486 A	19980428	18	High capacity ATM switch	370/395.71	370/380	

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Wireless Communications and Networking Conference, 2002. WCNC2002. 2002

Volume: 1, 17-21 March 2002

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Armitage, G.J.; Adams, K.M.;

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7 Design and implementation of ultra-low latency optical label switchir packet-switched WDM networks

Meagher, B.; Chang, G.K.; Ellinas, G.; Lin, Y.M.; Xin, W.; Chen, T.F.; Yang, X.; Chowdhury, A.; Young, J.; Yoo, S.J.; Lee, C.; Iqbal, M.Z.; Robe, T.; Dai, H.; Cl Y.J.; Way, W.I.;

Lightwave Technology, Journal of , Volume: 18 Issue: 12 , Dec 2000

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A complete set of VLSI circuits for ATM switching

Collivignarelli, M. Daniele, A. De Nicola, P. Licciardi, L. Turolla, M. Zappalorto, A.
Italtel-Settimo Milanese;*This paper appears in: Global Telecommunications Conference, 1994. GLOBECOM '94. 'Communications: The Global Bridge', IEEE*

Meeting Date: 11/28/1994 -12/02/1994

Publication Date: 28 Nov- 2 Dec 1994

Location: San Francisco, CA , USA

On page(s): 134-138 vol.1

References Cited: 7

INSPEC Accession Number: 5079720

Abstract:

The broadband services offered via the ATM-based B-ISDN range from high-speed data services to imaging services. A complete chip set for ATM switching system is presented. The VLSI components allow one to implement the most significant functions in an ATM node. Three chips are located in the exchange termination: the cell header processor that processes the ATM cells for label conversion, external to internal format translation and cell extraction and insertion, the policing unit that implements both the usage and the network parameter control functions, and the duplicated path recombining controller that duplicates and recombines respectively the input and output cell flow. The fourth component is the core of the ATM switching fabric: the broadband ATM switching element that switches the ATM cells according to the routing information written in the cell internal header, this component is presented in two different realisations (a CMOS low power 8×8, a BiCMOS 16×16). All the circuits are designed for an industrial environment and are inserted in the Italtel UTXC cross connect. System debugging, testability and controllability inspired the whole chip set design. Flexibility of specifications allows one to fit other applications and future development. High performance in terms of speed, low power dissipation, high integration density really stressed the technology of VLSI circuits.

Index Terms:

ATM cells ATM node ATM switching fabric ATM switching systems B-ISDN BiCMOS chip BiCMOS digital integrated circuits CMOS digital integrated circuits CMOS low power chip Italtel UTXC cross connect VLSI VLSI circuits asynchronous transfer mode broadband ATM switching element cell extraction cell flow cell header processor cell insertion cell recombination cell flow cell header processor cell insertion duplicated path recombining controller electronic switching systems exchange termination format translation network parameter control policing unit routing information system debugging usage parameter control ATM cells ATM node ATM switching fabric ATM switching systems B-ISDN BiCMOS chip BiCMOS digital integrated circuits CMOS digital integrated circuits CMOS low power chip Italtel UTXC cross connect VLSI VLSI circuits asynchronous transfer mode broadband ATM switching element cell extraction cell flow cell header processor cell insertion duplicated path recombining controller electronic switching systems exchange termination format translation network parameter control policing unit routing information system debugging usage parameter control

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Design and implementation of ultra-low latency optical label switching for packet-switched WDM networks

Meagher, B. Chang, G.K. Ellinas, G. Lin, Y.M. Xin, W. Chen, T.F. Yang, X. Chowdhury, A. Young, J. Yoo, S.J. Lee, C. Iqbal, M.Z. Robe, T. Dai, H. Chen, W. Way, W.I.

Telcordia Technol., Red Bank, NJ;

*This paper appears in: **Lightwave Technology, Journal of***

Publication Date: Dec 2000
 On page(s): 1978-1987
 Volume: 18, Issue: 12
 ISSN: 0733-8724
 References Cited: 10
 CODEN: JLTEDG
 INSPEC Accession Number: 6888891

Abstract:

An ultra-low latency, high throughput Internet protocol (IP) over wavelength division multiplexing (WDM) packet switching technology for next-generation Internet (NGI) applications has been designed and demonstrated. This method overcomes limitations of conventional optical packet switching, which require buffering of packets and synchronization of bits, and optical burst switching methods that require estimation of delays at each node and for each path. An optical label switching technique was developed to realize flexible bandwidth-on-demand packet transport on a reconfigurable WDM network. The aim was to design a network with simplified protocol stacks, scalability, and cost transparency. This network will enable the NGI users to send their data applications at gigabit/second access speed with low and predictable latency (μsec per switch node), with a system capacity of beyond multi-Tb/s. Packet forwarding utilizes WDM optical headers that are carried in-band on the same wavelength and modulated out-of-band in the frequency domain.

Index Terms:

Internet optical fibre subscriber loops packet switching protocols synchronisation telecommunication switching wavelength division multiplexing NGI users WDM optical headers WDM packet switching and width-on-demand packet transport data transparency frequency domain gigabit/second access speed high throughput Internet protocol modulated out-of-band next-generation Internet applications optical burst switching optical packet switching packet-switched WDM networks reconfigurable WDM network synchronization ultra-low latency optical label switching wavelength division multiplexing

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